UNITED STATES PATENT APPLICATION

FOR

A PHASE DETECTOR AND SIGNAL LOCKING SYSTEM CONTROLLER

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TITLE OF THE INVENTION

A PHASE DETECTOR AND SIGNAL LOCKING SYSTEM CONTROLLER

CROSS-REFRENCE TO RELATED APPLICATION

[0001] This application claims priority based on United States Provisional Patent Application Serial No. 60/287,229 filed on April 27, 2001.

FIELD OF THE INVENTON

[0002] This invention relates generally to a signal locking system controller and, more particularly, to a technique for controlling a digital phase-locked loop (PLL) for predictable modeling and dynamics.

BACKGROUND OF THE INVENTON

[0003] Signal locking systems typically rely on phase detectors in order to approximate the adjustment or gain factor to be applied to an output clock so as to coincide in time with an input reference signal clock. Typically, a phase difference between two clock sources of zero degrees is the design target in a standard phase-locked loop (PLL) system. PLL circuits can be implemented in either predominately digital or analog fashion, where the primary difference is in the way the output clock function is constructed. The analog PLL may, for example, employ a voltage-controlled oscillator (VCO), while a digital PLL may employ a digital accumulator circuit where the most significant bit (MSB) is typically used to form the output clock. In typical digital PLL circuits, the phase difference measurements are often limited by the frequency of the

digital system clock. For example, where the digital system clock is running at a frequency of 200MHz, the phase difference measurement resolution is only 5ns, or the period of the system clock. Thus, the minimum PLL system output jitter and wander, which are essentially system error factors, would also be 5ns in this example case.

[0004] FIG. 1 shows a type of phase detector, indicated by the general reference character **100**, that is capable of very good phase resolution. INPUT 1 signal **104** connects to the D-input of D-type flip-flop (DFF) **102**. INPUT 2 signal **106** connects to the clk-input of the DFF and the output **108** connects to the Q-output of the DFF. One of INPUT 1 or INPUT 2 may represent a feedback clock and the other a reference clock in a PLL system, for example. This circuit indicates the order of the signals based on the first transition edge (i.e., low-to-high or rising transition). The output **108** goes low if the INPUT 1 rising edge occurs after the INPUT 2 rising edge, but the output goes high if the INPUT 1 rising edge occurs prior to the INPUT 2 rising edge. This phase detection approach has the advantage of infinitesimally small timing resolution, but the disadvantage is that the gain, or the ratio of the increase in oscillator output frequency to the input phase difference, is very high and, as such, is very difficult to control.

[0005] The PLL system application requires a defined measurement of the input phase difference in order for the system to subsequently have a defined gain, bandwidth, and damping factor. The bandwidth is essentially the frequency range over which the PLL system allows stable operation. The damping factor indicates how well a system is damped and, as it follows, how much ringing is produced after an input signal disturbance. Common digital phase measurement techniques, such as those employing the standard type 4 phase and frequency

detector circuit are able to indicate the relative phase difference of two signals, but this approach is limited by the system clock and its general digital nature. As such, the resolution is insufficient to avoid excessive output jitter and wander in the phase-locked position, as described above. For the phase detector shown in FIG. 1, superior timing resolution is achieved, but the gain of this detector is not controllable and, thus, the associated PLL system dynamics of bandwidth and damping factor would also be uncontrollable.

[0006] As described, common phase detection approaches, particularly those used in digital-based signal locking systems like digital PLLs, typically suffer from either insufficient phase difference resolution for the application or uncontrollable gain.

[0007] It would be desirable to arrive at some way of providing phase difference information and control that would enable very high input phase difference resolution along with controllable PLL dynamics in an implementation that would remain reliable over the expected operating conditions and process variations.

SUMMARY OF THE INVENTION

[0008] A phase detector and a signal locking system controller, suitable for digital PLL systems, includes two different types of phase detectors, a synchronizing circuit, and a post processing and control unit. The first phase detector may be a common type 4 phase and frequency detector that is well known in the art. The first phase detector receives two input sources and outputs two phase indicator signals. The phase indicator signals couple to the synchronizing circuit along with a system clock and the synchronizing circuit outputs two synchronized phase indicator signals. The second phase detector also receives the two input sources and it generates an order indicator signal. The post processing and control unit receives the synchronized phase indicator signals, the order indicator signal, and an input source, and it outputs a phase measurement result signal. The post processing and control unit includes various circuits that allow for the system to use the information from the phase detectors and to apply a first gain factor when the input phase difference is relatively large and to apply a second gain factor when the input phase difference is relatively small. The first phase detector provides the phase difference information and enables control when the input sources are relatively far apart in phase and the second phase detector provides the signal order information and enables control when the input sources are relatively close in phase.

[0009] An advantage of the present invention is that it provides accurate and effective gain control and, as a result, also provides reliable modeling and system behavior.

[0010] Another advantage of the present invention is that the system performance is

largely independent of variations in operating temperature, supply voltage, or manufacturing process because of the digital nature of the design.

[0011] Another advantage of the present invention is that it allows for very fine input phase difference resolution as it is able to resolve time differences much less than the period of the system clock of the digital logic.

[0012] Yet another advantage of the present invention is that the post processing and control unit disallows conflict between the two types of phase detectors and this prevents dead-bands during the switching between control based on one phase detector to control based on the other.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate one or more embodiments of the invention and, together with the present description, serve to explain the principles of the invention.

[0014] In the drawings:

FIG. 1 is a schematic functional block diagram illustrative of a phase detector configuration in accordance with the prior art.

FIG. 2 is a schematic functional block diagram of a first portion of a specific embodiment of the present invention.

FIG. 3 is a timing diagram illustrative of the operation of a first portion of a specific embodiment of the present invention.

FIG. 4 is a schematic functional block diagram of a second portion of a specific embodiment of the present invention.

FIG. 5 is a timing diagram illustrative of the operation of the second portion of a specific embodiment of the present invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS OF THE INVENTION

[0015] A specific embodiment of the present invention is described herein in the context of a digital PLL system. Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and is not intended to be in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons having the benefit of this disclosure. Reference will now be made in detail to an implementation of the present invention as illustrated in the accompanying drawings.

[0016] In the interest of clarity, not all of the routine features of the implementations herein are described. It will of course be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system- and business-related constraints, and that these goals will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

[0017] FIG. 2 shows a schematic functional block diagram of a first portion of a specific embodiment of the present invention in the system indicated by the general reference character **200**. This first portion can include two different types of phase detectors and a synchronizing circuit. The first phase detector **230** can include D-type flip-flop (DFF) **202**, DFF **204**, and NAND-gate **208**. The second phase detector **232** can include DFF **206**. The synchronizing

circuit can include DFFs **210** and **212**. Flip flops 202, 204 and 206 use an asynchronous reset structure.

[0018] The positive voltage supply, VDD, can connect to the D-inputs of DFFs **202** and **204** and also to the reset-input of DFF **206**. The first input source **226**, INPUT A, can connect to the clk-inputs of DFFs **202** and **206**. The second input source **228**, INPUT B, can connect to the clk-input of DFF **204** and also to the D-input of DFF **206**. The first phase indicator signal **214**, UP, can connect to the Q-output of DFF **202**, to the first input of NAND-gate **208**, and to the D-input of DFF **210**. The second phase indicator signal **216**, DOWN, can connect to the Q-output of DFF **204**, to the second input of NAND-gate **208**, and to the D-input of DFF **212**. The active-low reset control signal **218**, RESETB, can connect to the reset-inputs of DFFs **202** and **204**. The system clock signal **234**, SYS CLK, can connect to the clk-inputs of DFFs **210** and **212**. The first synchronized phase indicator signal **222**, UP_SYNC, can connect to the Q-output of DFF **210** and the second synchronized phase indicator signal **224**, DOWN_SYNC, can connect to the Q-output of DFF **212**. The order indicator signal **220**, ADVB/RETARD, can connect to the Q-output of DFF **206**. Those of ordinary skill in the art will now realize that other logic structures can be built to achieve the same function as that described for first phase detector 230 and second phase detector 232.

[0019] Referring now to the timing diagram of FIG. 3 and viewing this diagram in conjunction with FIG. 2, the operation of the circuit will be described by way of example.

[0020] In the example, the first section of the timing diagram (the left half of the figure) shows an example case for a first operational mode of the controller where the input sources differ by a relatively large amount. This amount can typically be greater than the system clock signal (SYS CLK) period, but the circuit may detect this difference as relatively large in some cases when the difference is less that a SYS CLK period. In the first section, the first input source (INPUT A) is shown leading the second input source (INPUT B). Upon detection of the rising edge of INPUT A, the first phase indicator signal (UP) can go high (i.e., active). Upon detection of the rising edge of INPUT B, the second phase indicator signal (DOWN) can go high. The NAND-gate discharges the reset control signal (RESETB) and this can reset DFFs **202** and **204**, subsequently causing UP and DOWN to discharge (i.e., deactivate). It should be noted that the implementation may include additional delay to the RESETB signal in order to allow enough time to ensure the proper resetting of registers **202** and **204**. The first synchronized phase indicator signal (UP_SYNC) can become active upon the SYS CLK rising (i.e., first transition) edge while UP is high. The second synchronized phase indicator signal (DOWN_SYNC) can remain in a low state because DOWN was not high upon a SYS CLK rising edge. Thus, the synchronizing circuit was not able to detect the second phase indicator signal as active. The UP_SYNC can indicate that INPUT A leads INPUT B by an amount proportional to the high time of the first synchronized phase indicator signal. The order indicator signal (ADVB/RETARD) can remain low because DFF **206** can detect INPUT B as low upon the rising edge of INPUT A.

[0021] The second section of the timing diagram (the right half of the figure) shows an example case for a second operational mode of the controller where INPUT A leads INPUT B by

only a very small amount, as related to the SYS CLK period. Again, UP can go high upon the rising edge of INPUT A and DOWN can, similarly, go high upon the rising edge of INPUT B. The RESETB signal can subsequently go low to activate the resetting mechanism of registers **202** and **204**, and this can discharge both UP and DOWN. Because neither UP nor DOWN are active upon a rising edge of SYS CLK, UP_SYNC and DOWN_SYNC can remain low, indicating that the synchronizing circuit has not detected an active phase indicator signal. Again, ADVB/RETARD can remain low because DFF **206** can detect INPUT B as low upon the rising edge of INPUT A.

[0022] FIG. 4 shows a schematic functional block diagram of a second portion of a specific embodiment of the present invention in the system indicated by the general reference character **400**. This second portion can include a synchronous signal latch **402**, a first multiplexer **406**, an edge detection block **404**, a first register (DFF) **408**, a second register (DFF) **414**, a programmable storage unit **416**, a second multiplexer **410**, and a divider **412**.

[0023] The first synchronized phase indicator signal **222**, UP_SYNC, can connect to the A-input of the synchronous signal latch **402**. The second synchronized phase indicator signal **224**, DOWN_SYNC, can connect to the B-input of the synchronous signal latch and also to the second input of the first multiplexer **406**. The order indicator signal **220**, ADVB/RETARD, can connect to the first input of the first multiplexer. The first input source **226**, INPUT A, can connect to the input of the edge detection block **404**. The edge detection control signal **420**, EDGE_DET, can connect to the output of the edge detection block, to the reset-input of the synchronous signal latch, and to the clk-inputs of DFFs **408** and **414**. The first multiplexer

selection control signal **418**, MUX1_SEL, can connect to the output of the synchronous signal latch, to the selection input of the first multiplexer **406** and also to the D-input of DFF **408**. The first multiplexer output signal **422**, MUX1_OUT, can connect to the D-input of DFF **414**. The second multiplexer selection control signal **430**, MUX2_SEL, can connect to the Q-output of DFF **408** and to the selection input of the second multiplexer **410**. The programmable storage unit **416** output can couple to the first input of the second multiplexer and a default gain value can couple to the second input of the second multiplexer. The second multiplexer output signal **424**, MUX2_OUT, can connect to the A-input of divider **412**. The phase result indicator signal **426**, PH_RES, can connect to the Q-output of DFF **414** and also to the B-input of divider **412**. The phase measurement result signal **428**, FINAL_PM_RES, can connect to the C-output of the divider.

[0024] Referring now to the timing diagram of FIG. 5 and viewing this diagram in conjunction with FIG. 4, the operation of the circuit will be described by way of continuing the example above. In FIG. 5, the system clock signal (SYS CLK), the first input source (INPUT A), the first synchronized phase indicator signal (UP_SYNC), and the second synchronized phase indicator signal (DOWN_SYNC) are all carried over from the example case illustrated in FIG. 3.

[0025] In FIG. 5, the first section of the timing diagram (the left half of the figure) continues the example case for a first operational mode of the controller where the input sources differ by a relatively large amount.

[0026] The first multiplexer selection control signal (MUX1_SEL) can go high upon the rising edge of UP_SYNC by the action of the synchronous signal latch **402**. The edge detection control signal (EDGE_DET) can go high upon the second transition (i.e., falling) edge of the first input source (INPUT A). EDGE_DET can then reset MUX1_SEL and also bring the second multiplexer selection control signal (MUX2_SEL) high upon its rising edge through the DFF **408** operation. The first multiplexer output signal (MUX1_OUT) can remain low because ADVB/RETARD is low while MUX1_SEL is low and DOWN_SYNC is low while MUX1_SEL is high. The second multiplexer output signal (MUX2_OUT) can switch to the default gain value (logic high) upon MUX2_SEL going high. The phase result indicator signal (PH_RES) can remain low because MUX1_OUT remains low. The phase measurement result signal (FINAL_PM_RES) can switch to the "-F" value because the B-input of the divider **412** (PH_RES) is low and the A-input of the divider is "1" (i.e., logic high level). This represents the coarse control needed by the overall PLL system as part of the first operational mode of the controller.

[0027] The second section of the timing diagram (the right half of FIG. 5) continues the example case for a second operational mode of the controller where INPUT A leads INPUT B by only a very small amount, as related to the SYS CLK period.

[0028] UP_SYNC can remain low because the first phase indicator signal is not recognized by the synchronizing circuit. Similarly, and as described above, DOWN_SYNC can also remain low. MUX1_SEL can remain low because the synchronous signal latch **402** can detect UP_SYNC and DOWN_SYNC as both low. The edge detection block **404** can produce a

high on EDGE_DET upon the falling edge of INPUT A. MUX1_OUT can remain low because ADVB/RETARD is low and MUX1_SEL is low. MUX2_OUT can switch to the gain combiner value (i.e., N-bit register value) upon MUX2_SEL going low. The phase result indicator signal (PH_RES) can remain low because MUX1_OUT remains low. The phase measurement result signal (FINAL_PM_RES) can switch to the "-F/(N-BIT REG)" value because the B-input of the divider **412** (PH_RES) is low and the A-input of the divider is the gain combiner value, "N-BIT REG". This represents the more fine tuning control needed by the overall PLL system as part of the second operational mode of the controller.

[0029] The example shows only two input sources, but as it is clear to one skilled in the art, more than two signals, with or without additional phase detector implementations, could be included in the system. Also, while the example described input sources with the same frequency, the source signals could also differ in frequency. The nature and implementation of the phase measurement result signal could also be altered to accommodate different system applications.

[0030] The coupling of certain signals to certain functional blocks could also be altered without changing the scope of the invention. For example, in FIG. 4, the first synchronized phase indicator signal instead of the second synchronized phase indicator signal might be coupled to the first multiplexer. Or, the second input source instead of the first input source might be coupled to the edge detection block. Also, many of the components described are representative of the various functional blocks that may be part of a given implementation;

however, other implementations using different functional block representations could also be realized by those of ordinary skill in the art.

[0031] While embodiments and applications of this invention have been shown and described, it would be apparent to those of ordinary skill in the art having the benefit of this disclosure that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.